REMARKS

Claims 1-28 remain in the application. Claims 1, 7, 12, 19, and 24 have been amended.

Claim Rejections under 35 U.S.C. § 102

Claims 1-28 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,790,822 to Sheaffer et al. ("Sheaffer"). Claims 1, 2, 7, 8, 12, 13, 19, 20, 24, and 25 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,471,593 to Branigin ("Branigin").

According to an embodiment of the present invention, an instruction cache is provided to store instructions that have been "steered" into it based on a set of execution units that the instruction requires. For example, looking at Fig. 4 of the present application, a pre-steered instruction cache 148 is provided with a number of bins. The bins are associated to particular execution units such as an integer execution unit 143x, a floating point execution unit 143y and a memory execution unit 143z. By storing the decoded instructions in a cache in this manner, the instructions may be quickly issued to the appropriate execution unit (including, for example, the reservation station associated with the execution unit) resulting in an increase in processor performance. Claims 1, 7, 12, 19, and 24 have been amended to bring out the feature of the present invention of issuing the instructions from the instruction cache.

Scheaffer refers to system for providing a re-ordered instruction cache in a pipelined microprocessor. Referring to Fig. 1 in Scheaffer, decoded instructions are provided to a re-order unit 134 that orders the instructions in such a manner so as to separate data dependencies and to separate instructions that are to be sent to the same execution unit (see Col. 5, line 50 to Col. 6, line 5). The resulting re-ordered instructions are stored in the instruction cache 136 in such a manner (see Figs. 1 and 4 and Col. 6, lines 6-18). Thus, according to Scheaffer, instructions in the instruction cache are not steered into the cache according to a particular one or cluster of the

execution units as recited in each of the pending claims. Instead, they are steered into the instruction cache so as to specifically space instructions for the execution units apart from one another.

Branigin describes in Fig. 5 a processor with Tomasulo's algorithm. As shown in Fig. 5, instructions are decoded and then immediately transmitted to reservation stations. As indicated in Scheaffer at Col. 4, lines 28-35, the reservation station makes instructions ready and schedules them for execution by the associated execution unit. There does not appear to be an instruction cache shown in Fig. 5 where instructions are steered into it according to a particular one or cluster of execution units that the instructions require as called for in each of the pending claims. Moreover, with respect to claim 7, there is no teaching or discussion in Branigan as to the scheduling of instructions to avoid pipeline stall before steering them into the instruction cache as called for by this claim.

Since features of each of the pending claims are neither taught nor suggested by the Scheaffer or Branigin references, reconsideration and withdrawal of the rejection of claims 1-28 under 35 U.S.C. § 102(b) is respectfully requested.

CONCLUSION

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4255 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,
KENYON & KENYON

Dated: 5/6/03

By: Shawn O'Dowd

Shawn W. O'Dowd
Reg. No. 34,687

KENYON & KENYON
1500 K Street, NW
Suite 700
Washington DC, 20005
(202) 220-4200 telephone
(202) 220-4201 facsimile
DC:452979v1

SJ01 26244 v 1